



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	09/881934	Docket Number	MIPS.0173-00-US
Filed	02/13/04	Group Art Unit	2188
Examiner	KEVIN L. ELLIS	Customer No.	23669
Application Title	METHODS AND APPARATUS FOR ALLOCATING AND DE-ALLOCATING CONSECUTIVE BLOCKS OF MEMORY IN BACKGROUND MEMORY MANAGEMENT		
First Named Inventor	ENRIQUE MUSOLL		

### INFORMATION DISCLOSURE STATEMENT TRANSMITTAL

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Attached hereto is Form PTO-1449 listing documents believed relevant to the subject application. It is respectfully requested that the examiner review the information disclosed herein in detail, independently evaluate each item carefully in the consideration of the pending claims, and return an initialed copy of each form to the undersigned practitioner.

This disclosure statement should not be construed as a representation that a search has been made, that no other material information as defined in 37 CFR 1.56(a) exists, or as an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b) or is available as a reference under 35 U.S.C. §102 *et seq.* Applicant reserves the right to swear behind or otherwise disprove the allege "prior" nature of any art cited should the facts support and the situation warrant such an action.

It is believed that this disclosure complies with the requirements of 37 CFR 1.56, 1.97, and 1.98, and the Manual of Patent Examining Procedures §609. If for some reason the examiner considers otherwise, it is respectfully requested that the undersigned be called so that any deficiencies can be remedied.

Some of the enclosed documents may have markings thereon. No significance is intended to be attached to the markings.

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Respectfully submitted,  
**HUFFMAN PATENT GROUP, LLC**

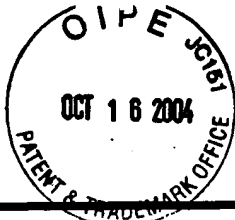
By \_\_\_\_\_

**RICHARD K. HUFFMAN**

Reg. No. 41,082

Tel.: (719) 575-9998

Date 10/16/04



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Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
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				Examiner Name	KEVIN L. ELLIS
				Attorney Docket Number	MIPS.0173-00-US
Sheet	1	of	3		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
		US-4200927	04-29-1980	Hughes et al.	
		US-6535905	03-18-2003	Kalafatis et al.	
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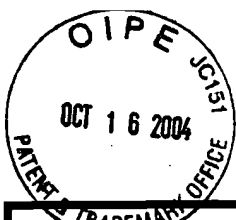
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

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### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	AA	YAMAMOTO, WAYNE. <i>An Analysis of Multistreamed, Superscalar Processor Architectures</i> . University of California Santa Barbara Dissertation. December 1995. Santa Barbara, US.	
	AB	YAMAMOTO et al. "Increasing Superscalar Performance Through Multistreaming." <i>Parallel Architectures and Compilation Techniques (PACT '95)</i> . 1995	
	AC	<i>The PowerPC Architecture: A Specification for a New Family of RISC Processors</i> . 2 <sup>nd</sup> Ed. May 1994. pp. 70-72. Morgan Kaufmann. San Francisco, US.	
	AD	<i>MC68020 32-Bit Microprocessor User's Manual</i> . 3 <sup>rd</sup> Ed.. 1989. pp. 3-125, 3-126, and 3-127. Prentice Hall, NJ, US.	
	AE	POTEL, M. J. "Real-Time Playback in Animation Systems." <i>Proceedings of the 4<sup>th</sup> Annual Conference on Computer Graphics and Interactive Techniques</i> . 1977. pp. 72-77. San Jose, CA, US.	
	AF	<i>ARM Architecture Reference Manual</i> . 1996. pp. 3-41, 3-42, 3-43, 3-67, and 3-68. Prentice Hall, NJ, US.	
	AG	<i>ESA/390 Principles of Operation</i> . IBM Online Publications Center Reference Number SA22-7201-08. Table of Contents and paras. 7.5.31 and 7.5.70. IBM Corporation. Boulder, CO, US.	
	AH	<i>MC88110 Second Generation RISC Microprocessor User's Manual</i> . 1991. pp. 10-66, 10-67, and 10-71. Motorola, Inc.	
	AI	DIEFENDORFF, KEITH ET AL. "Organization of the Motorola 88110 Superscalar RISC Microprocessor." <i>IEEE Journal of Microelectronics</i> . April 1992. pp. 40-63. Vol. 12, No. 2. IEEE. New York, NY, US.	
	AJ	KANE, GERRY. <i>PA-RISC 2.0 Architecture</i> . 1996, pp. 7-106 and 7-107. Prentice Hall. NJ, US.	
	AK	DIEFENDORFF, KEITH ET AL. "Altivec Extension to PowerPC Accelerates Media Processing." <i>IEEE Journal of Microelectronics</i> . Vol. 20, No. 2 (2000): pp. 85-95	
	AL	GRUNEWALD, WINFRIED ET AL. "Towards Extremely Fast Context Switching in a Block Multithreaded Processor." <i>Proceedings of EUROMICRO 22</i> , 1996. pp. 592-599	
	AM	BRADFORD, JEFFREY ET AL. "Efficient Synchronization for Multithreaded Processors." <i>Workshop on Multithreaded Execution, Architecture, and Compilation</i> . Jan-Feb 1998. pp. 1-4	
	AN	PAI, VIJAY ET AL. "An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors." <i>Proceedings of ASPLOS-VII</i> , Oct. 1996: pp. 12-23, ACM, Inc.	

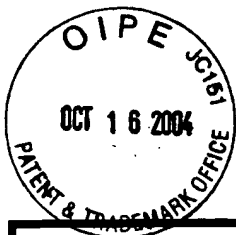
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	AO	YOAZ ET AL. "Speculation Techniques for Improving Load Related Instruction Scheduling." 1999. Pages 42-53, IEEE.	
	AP	KESSLER, R. E. "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 MHz." August 1998.	
	AQ	DONALDSON ET AL. "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance." 26 <sup>th</sup> Hawaii Conference on Systems Sciences. Vol. 1. 1993. Pages 448-456.	
	AR	NEMIROVSKY ET AL. "DISC: Dynamic Instruction Stream Computer." ACM. 1991. Pages 163-171	
	As	MUSOLL ET AL., "Mechanism to Activate a Context When No Stream is Running in a Multi-Streaming Processing Core," April 16, 2001, Disclosure Document #492431, USPTO	
	AT	MUSOLL ET AL., "Mechanism for Allowing a Limited Packet Head and/or Tail Growth Without Moving the Packet to a Different Memory Location," April 16, 2001, Disclosure Document #492429, USPTO	
	AU	MUSOLL, ENRIQUE, "Functional Validation of a Packet Management Unit," May 18, 2001, Disclosure Document #494011, USPTO	
	AV	MELVIN ET AL., "Extended Instruction Set for a Packet Processing Applications," July 5, 2001, Disclosure Document #496559, USPTO	
	AW	MUSOLL ET AL., "Mechanism to Overflow Packets to a Software Controlled Memory When They Do Not Fit into a Hardware Controlled Memory," July 3, 2001, Disclosure Document #496391, USPTO	

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